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EXAMINER	
OSORIO, RICARDO	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/809,925	YAMAZAKI, HIROSHI	
	Examiner	Art Unit	
	RICARDO L. OSORIO	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/4/2008 has been entered.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by Go (US 6,320,566 B1) hereinafter referred to as Go '566.

3. With regard to claim 11, Go '566 discloses **a timing controller** (see column 4 line 10, "clock signal generator") **for a liquid crystal display device,** (see column 4 lines 1-2) **characterized in that data signals of odd-number dots and data signals of even-number dots** (see column 4, lines 20-24) **are output every horizontal line** (see FIG. 6A and 6B described in column 2, lines 46-48 in conjunction with FIG. 10 further described at column 6, lines 20-25) **while displacing the phase between the data signals of the odd-number dots and even-number dots by 180 degrees.** (see FIG. 10 and elements 140 and 150 further described as

high and low video data at column 7, lines 1-16 and as illustrated in FIGs 10-12; additionally see column 6, lines 20-25).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Go, United States Patent Number 6,320,566 B1, Date of Patent: November 20, 2001 (hereinafter referred to as "Go '566") and further in view of Misawa et al., United States Patent Number: 5,616, 936, Date of Patent: April 1, 1997 (hereinafter referred to as "Misawa '936").

6. With regard to claim 1, Go '566 discloses **a liquid crystal display device** (see column 1, lines 10-11) **comprising: a liquid crystal display panel;** (see column 1, lines 34-47) **a plurality of data driver integrated circuits (ICs) for driving data lines of the liquid crystal display panel;** (see column 3, lines 33-38) **a first clock signal line** (see column 4, line 11, "first clock signal" furthermore see FIG. 10 element labeled "FD1" and column 6 lines 21 "first clock signal FD1) **for transmitting a first clock signal to the plurality of data driver ICs** (see column 4, lines 22-25) **a second clock signal line** (see column 4, line 11, "second clock signal" furthermore see FIG. 10 element labeled "FD2" and column 6 lines 22 "first clock signal FD2)

which is equipped in parallel with the first clock signal line (see FIGs. 10 and 12, clock signal lines FD1 and FD2 are drawn in parallel) **and transmits a second clock signal which is in reverse relation with the first clock signal;** (see column 4, lines 10-13, describing the signals having a180 degree phase difference, furthermore, see FIG 11, showing the phase difference) **and a timing controller for outputting the first and second clock signals to the first and second clock signal lines respectively;**(see column 4, lines 10-13 describing a "clock signal generator"; furthermore described in detail at column 6, lines 20-21 described as a "controller IC 100")

7. However, Go '566 fails to teach **a load means for making the load capacitance of the second clock signal line equal to or substantially equal to the load capacitance of the first clock signal line.**

8. However, Misawa '936 teaches **a load means for making the load capacitance of the second clock signal line equal to or substantially equal to the load capacitance of the first clock signal line**. (see column 20, lines 15-25, the "source line driving circuit" performs this function).

9. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the source line driving circuit as disclosed in Misawa '936 into the liquid crystal display device of Go '566 because, as disclosed in column 12 lines 17-46 of Misawa '936, equalizing the capacitance reduces the added noise and improves picture quality, both of which are consistently progressive goals within the art

10. With regard to claim 5 as dependent on claim 1, Go '566 discloses **a data signal line for odd-number dots** (see column 4, lines 20-24, "odd data lines") **for transmitting data signals of**

odd-number dots (pixel electrodes 26 are attached to the odd data lines) **and a data signal line for even-number dots** (see column 4, lines 20-24, "even data lines") **for transmitting data signals of even-number dots** (pixel electrodes 26 are attached to the odd data lines) **are equipped, and the timing controller outputs the data signals of the odd-number dots and the data signals of the even-number dots every horizontal line** (see FIG. 6A and 6B described in column 2, lines 46-48 in conjunction with FIG. 10 further described at column 6, lines 20-25) **while displacing the phase between the data signals of the odd-number and even-number dots by 180 degrees,** (see column 6, lines10-14 in conjunction with lines 20-28) **and the data driver ICs input the first and second clock signals** (see column 6, lines 19-25)**, latch the data signals of the odd-number dots with the first clock signal and latch the data signals of the even-number dots with the second clock signal** (see column 6, lines 20-28).

11. Claims 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Go, United States Patent Number 6,320,566 B1, Date of Patent: November 20, 2001 (hereinafter referred to as "Go '566") and further in view of Jeon et al., (US 6,690,347 B2) hereinafter referred to as "Joen '347".

12. With regard to claim 7 as amended, Go '566 discloses **a liquid crystal display device** (see column 1, lines 10-11) **comprising: a liquid crystal display panel;** (see column 1, lines 34-47) **a plurality of data driver ICs for driving data lines of the liquid crystal display panel;** (see column 3, lines 33-38) **a first clock signal line** (see column 4, line 11, "first clock signal" furthermore see FIG. 10 element labeled "FD1" and column 6 lines 21 "first clock signal FD1) **for transmitting a first clock signal to the plurality of data driver ICs** (see column 4, lines

22-25) **a second clock signal line** (see column 4, line 11, "second clock signal" furthermore see FIG. 10 element labeled "FD2" and column 6 lines 22 "first clock signal FD2) **which is equipped in parallel with the first clock signal line** (see FIGs. 10 and 12, clock signal lines FD1 and FD2 are drawn in parallel) **and transmits a second clock signal which is in reverse relation with the first clock signal;** (see column 4, lines 10-13, describing the signals having a180 degree phase difference, furthermore, see FIG 11, showing the phase difference) **and a timing controller for outputting the first and second clock signals to the first and second clock signal lines respectively;**(see column 4, lines 10-13 describing a "clock signal generator"; furthermore described in detail at column 6, lines 20-21 described as a "controller IC 100") **wherein each of the data driver ICs input the first and second clock signals, and can selectively latch data signals with the first or second clock signal.** (see column 4, lines 20-28 describing latching data signals and gates to selectively latch to even or odd lines).

1. However, Go '566 does not explicitly teach **a selection signal, select the first or second clock signal based on the selection signal**. In the same field of endeavor, Joen '347 clearly teaches **a selection signal, select the first or second clock signal based on the selection signal** (see Joen '347 at but not limited to, column 7, lines 35-49 describing a selection start signal as applied and also column 10, lines 23-56).

2. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the selection signal as taught by Joen '347 into the display device of Go '566 because both are within the same field of endeavor, and furthermore, because the design as taught by Joen '347 minimizes the number of external

connection terminals through its use of two clock signals in block operation (see Joen '347 at column 2, lines 48-end) a common goal within this art.

3. Claims 9 and 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Go '566 and further in view of Jeong (US 6,335,721 B1) hereinafter referred to as Jeong '721.

4. With regard to claim 9, Go '566 discloses **a data driver IC** (see column 1, line 52 "data driver IC 11") **for a liquid crystal display device,** (see column 1, lines 10-11). **a first data latch** (see FIG. 12 element 200, further described at column 6, lines 37-47) **that inputs a first clock signal** (see FIG. 12, FD1) **and latches data signals of odd-number dots with the first clock signal** (see column 6, lines 37-65)**; and data latch** (see FIG. 12, element 200) **that inputs a second clock signal in reverse relation with the first clock signal** (see FIG. 12, FD2, and as described at column 6, lines 37-65, further illustrated at FIG. 11) **and latches data signals of even-number dots with the second clock signal**(see FIG. 12, and further described in column 6, lines 37-65)**.** Go '566 does not explicitly teach **a second data latch.**

5. In the same field of endeavor, Jeong '721 clearly teaches **a second data latch** (see FIG. 4 illustrating first and second latch and FIG. 5, further described at column 3, lines 1-40 and column 4, lines 15-40)**.**

6. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the second data latch as taught by Jeong '721 into the device of Go '566 because both are within the same field of endeavor, and furthermore, because the design of Jeong '721 improves image quality by buffering negative and positive polarity video signals (see Jeong '721, column 2, lines 53-57).

7. Furthermore, Go '566 does not explicitly teach of **a sampling memory that samples and stores said data signals received from the first and the second data latches**.

8. Jeong '721 teaches a sampling memory (Fig. 2, characters 56 and 70) that sample and store inverse polarity data signals received from fist and second data latches (see col. 1, line 55-col. 2, line 5).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the sampling memory as taught by Jeong '721 into the device of Go '566 because both are within the same field of endeavor, and furthermore, because sample and hold circuits are overwhelmingly known in the art of display devices for sampling video signals to a form that can be appropriately sent to the LCD cells.

9. With regard to claim 10, Go '566 clearly teaches **a data driver IC** (see Go '566 column 1, line 52 "data driver IC 11") **for a liquid crystal display device** (see Go '566 column 1, lines 10-11)**, characterized in that the data driver IC inputs a first clock signal** (see Go '566 FIG. 12, FD1, and as described at column 6, lines 37-65, further illustrated at FIG. 11)**and a second clock signal in reverse relation with the first clock signal** (see Go '566 FIG. 12, FD2, and as described at column 6, lines 37-65, further illustrated at FIG. 11). **a selection signal** (see Jeong '721 column 4 lines 43-end and continued at column 5, lines 1-8)**, select the first or second clock signal based on the selection signal, and a can selectively latch data signals with the first or second clock signal** (see Jeong '721 column 4 lines 61-end and continued at column 5, lines 1-8)**.**

10. Claim12 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Go '566" and further in view of Ogata et al., Japanese Patent Number JP 407329337A. Hereinafter referred to as "Ogata".

11. With regard to claim 12, Go '566 discloses **a timing controller** (see column 4, lines 10-13 describing a "clock signal generator"; furthermore described in detail at column 6, lines 20-21 described as a "controller IC 100") **for a liquid crystal display device** (see column 1, lines 10-11) However, Go '566 fails to discloses **a data signal of a dot is consisted of a plurality of bits, and output pins for data signals are arranged so that the data signal of an odd-number dot of each bit of each color and the data signal of an even-number dot of the same bit are adjacent to each other.**

12. Ogata discloses **a data signal of a dot is consisted of a plurality of bits** (see abstract discussing bits)**, and output pins** (see demonstrative FIG 1 illustrating odd lines 1, 3…n-1 adjacent to even lines 2, 4… n-1) **for data signal of an odd-number dot of each bit of each color** (see abstract "data signal having odd bits") **of each bit** (see abstract "of one line") **and the data signal of an even-number dot** (see abstract "data signal having even bits") **of the same bit** (see abstract "of one line") **are adjacent to one another** (see demonstrative FIG 1 illustrating odd lines 1, 3…n-1 adjacent to even lines 2, 4… n-1)**.**

13. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the display device of Go '566 into the data signal line arrangement of Ogata because as disclosed in Ogata, the arrangement "reduces the capacity of power source" and "prevents the decrease of image quality level."

13. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Go '566 and Misawa '936 as applied to claim 1 above, and further in view of Toyoshima et al., United States Patent, Patent Number US 6,795,049 B2, Date of Patent: September 21, 2004 (hereinafter referred to as "Toyoshima '049").

14. With regard to claim 2, Go '566 in view of Misawa '936 teaches **the liquid crystal display device according to claim 1.** However, Go '566 in view of Misawa '936 fail to teach the **load means is constructed by equipping dummy terminals to the data driver ICs, and connecting the second clock signal line to the dummy terminals.**

15. However, Toyoshima '049 discloses **the load means is constructed by equipping dummy terminals** (column 5, lines 31-33, describing dummy element) **to the data driver ICs** (see FIG 4, further described in column 7, lines 43-59)**, and connecting the second clock signal line to the dummy terminals** (see FIG 4. further described in column 7, lines 43-59; the second clock line is connected to the dummy lines)**.**

16. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the dummy terminal configuration of Toyoshima '049 into the display device of Go '566 in view of Misawa '936 because Toyoshima '049 provides for stable operation of the display device and a reduced area of elements outside of the display region (see column 1, lines 55-60).

17. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Go '566 in view of Misawa '936 as applied to claim1 above, and further in view of Drake et al., United States Patent, Patent Number 6,339,413 B1, Date of Patent: January 15, 2002 (hereinafter referred to as Drake '413).

18. With regard to claim 3 Go '566 in view of Misawa '936 discloses **the liquid crystal display device according to claim 1,** However, Go '566 in view of Misawa '936 fails to teach **the load means is constructed by containing a capacitor in a terminating circuit.**

19. In the same field of endeavor, Drake '413 clearly teaches **the load means is constructed by containing a capacitor in a terminating circuit** (see Figure 6 element 108 used to reduce or eliminate noise and is connected to ground, furthermore, see column 10, lines 37-40).

20. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate display device of Go '566 in view of Misawa '936 into the drive circuit of Drake '413 because the design of Drake '413 reduces noise in the circuit (see column 10, lines 37-40).

21. With regard to claim 4 and as dependent on claim 3, Misawa '936 discloses having another capacitance value having the **same capacitance value as the input capacitance of the first clock signal input terminals of the data driver ICs.** Namely, Misawa '936 clearly discloses equalizing the capacitance of the two clock signal lines with the signal bus, and therefore equating the two clock lines. Therefore it would have been obvious to one having ordinary skill in the art at the time of invention to have combined the terminal capacitor of Drake '413 into the equalizing capacitance design of Misawa because such a design would further reduce the noise in the circuit (see column 10, lines 37-40 of Drake '413).

22. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over "Go '566" in view of Misawa '936 and further in view of Ogata et al., Japanese Patent Number JP 407329337A. Hereinafter referred to as "Ogata".

23. With regard to claim 6, Go '566 discloses **the liquid crystal display device according to claim 5, wherein a data signal of a dot is consisted of a plurality of bits and a timing controller** (see column 4, lines 10-13 describing a "clock signal generator"; furthermore described in detail at column 6, lines 20-21 described as a "controller IC 100") **for a liquid crystal display device** (see column 1, lines 10-11). However, neither Go '566, nor Misawa '936 teach **output pins for data signals are arranged so that the data signal of an odd-number dot of each bit of each color and the data signal of an even-number dot of the same bit are adjacent to each other.**

24. Ogata discloses **data signal of an odd-number dot of each bit of each color** (see abstract "data signal having odd bits") **of each bit** (see abstract "of one line") **and the data signal of an even-number dot** (see abstract "data signal having even bits") **of the same bit** (see abstract "of one line") **are adjacent to one another** (see demonstrative FIG 1 illustrating odd lines 1, 3…n-1 adjacent to even lines 2, 4… n-1).

25. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the display device of Go '566 and Misawa '936 into the data signal line arrangement of Ogata because as disclosed in the purpose portion of the abstract of Ogata, the arrangement "reduces the capacity of power source" and "prevents the decrease of image quality level."

26. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Go '566 in view of Joen '347 as applied to claim 7 above, and further in view of Ogata.

27. Regarding claim 8 as amended, Go '566 in view of Joen '347 clearly teaches **the liquid crystal display device according to claim 7** (see above). Go '566 in view of Joen '347 does not

teach **a data signal of a dot is considered of a plurality of bits, and the data driver IC has input pins for data signals arranged so that the data signal of an odd-number of dot of each color and the data signal of an even-number dot of the same bit are adjacent to each other.**

28. Ogata discloses **a data signal of a dot is consisted of a plurality of bits** (see abstract discussing bits)**, and output pins** (see demonstrative FIG 1 illustrating odd lines 1, 3…n-1 adjacent to even lines 2, 4… n-1) **for data signal of an odd-number dot of each bit of each color** (see abstract "data signal having odd bits") **of each bit** (see abstract "of one line") **and the data signal of an even-number dot** (see abstract "data signal having even bits") **of the same bit** (see abstract "of one line") **are adjacent to one another** (see demonstrative FIG 1 illustrating odd lines 1, 3…n-1 adjacent to even lines 2, 4… n-1)**.**

29. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the display device of Go '566 in view of Joen '347 into the data signal line arrangement of Ogata because as disclosed in Ogata, the arrangement "reduces the capacity of power source" and "prevents the decrease of image quality level."

Response to Arguments

Applicant's arguments filed 4/28/2008 have been fully considered but they are not persuasive.

Applicant traverses the rejection of claim 11 as being anticipated by Go and argues that Go fails to disclose that "a timing controller displaces the phase between the data signals of the odd-number dots and the even number dots by 180 degrees". Examiner respectfully disagrees. As addressed in the Final Action, Go clearly discloses this limitation at least at column 6, lines 20-25. Furthermore, Examiner directs the Applicant to lines 20-64 further describing lines D1, D3, and D5 as odd data lines connected to first clock signal FD1, and D2, D4, and D6 as even data lines connected to FD2 wherein the phase of the signals applied to the odd and even data lines are 180-degrees apart. Therefore, claim 11 stands as rejected.

Applicant traverses the rejection of claims 1 and 5 as being unpatentable over Go in view of Misawa and argues that these two references do not disclose "a liquid crystal display device with first and second clock signal lines that are equipped in parallel and have a load capacitance that are equal or substantially equal by equipping the load means." Examiner respectfully disagrees. As addressed in the Final Action, Go in view of Misawa clearly teaches the limitation and as described by Applicant, lines 218 and 219 as described by Misawa have load capacitances that are substantially equal. The Misawa teaching although describing the lines crossing to keep equidistant from the video signal line, does not mention the lines intersect and therefore a twisting helical nature is presumed from the teaching to provide for normal functioning. Therefore, claims 1 and 5 stand rejected.

Regarding Applicant's argument that claim 1 encompasses the ability to adjust the load capacitance by the load means so as to have load capacitances that are equal or substantially equal. Examiner respectfully disagrees. The load means' adjustability has not been claimed in claim 1 and therefore this assertion has no basis. Therefore, claim 1 stands as rejected.

Applicant traverses the rejection of claim 7 as being unpatentable over Go in view of Jeon and argues that these two references fail to disclose "a selection signal that is used to select the first or second clock signal." Examiner respectfully disagrees. As clearly described in the Final Action, the combination of selection signal as taught by Jeon with the clock signal lines of Go would be obvious to one of ordinary skill in the art for the commonly understood benefits of reduction of external connection signals as taught by Jeon at column 2, lines 48-end. Therefore claim 7 stands as rejected.

Applicant traverses the rejection of claim 9 as being unpatentable over Go in view of Jeong and argues that the combination does not disclose "a sampling memory that samples and stores data signals". As described above, amended claim 9 will require further search and consideration.

Applicant traverses the rejection of claim 10 as being unpatentable over Go in view of Jeong and argues that the combination does not disclose "a selection signal which is used as the basis for selecting a first or second clock signal." Examiner respectfully disagrees. As indicated in the Final Action, Jeong clearly teaches the data latch and multiplexer as taught at column 4, lines 61-end and continued at column 5, lines 1-8. The device in combination with Go clearly would allow for selecting a first or second clock signal as described in the Final Action. Therefore, claim 10 stands as rejected.

Applicant traverses the rejection of claim 12 as being unpatentable over Go in view of Ogata and argues that the combination does not disclose "a dot consists of a plurality of bits." Examiner respectfully disagrees. As clearly described in the Final Action, Ogata teaches a data signal having odd bits and another signal line having even bits. Therefore the data signal corresponds to the dot and the bits in Ogata are congruent to the bits in the current application. Applicant further argues that Go in view of Ogata does not disclose "the output pin for a bit of a color of an odd-number dot is adjacent to an output pin of the same bit of the same color of an even-number dot." Examiner respectfully disagrees. As described in the Final Action, Ogata clearly depicts the adjacency as claimed in claim 12 at least at the demonstrative FIG. 1 illustrating parallel odd lines adjacent to even lines. Therefore, claim 12 stands as rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICARDO L. OSORIO whose telephone number is (571) 272-7676. The examiner can normally be reached on MONDAY-THURSDAY 7:00 am-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RICARDO L OSORIO/
Primary Examiner, Art Unit 2629